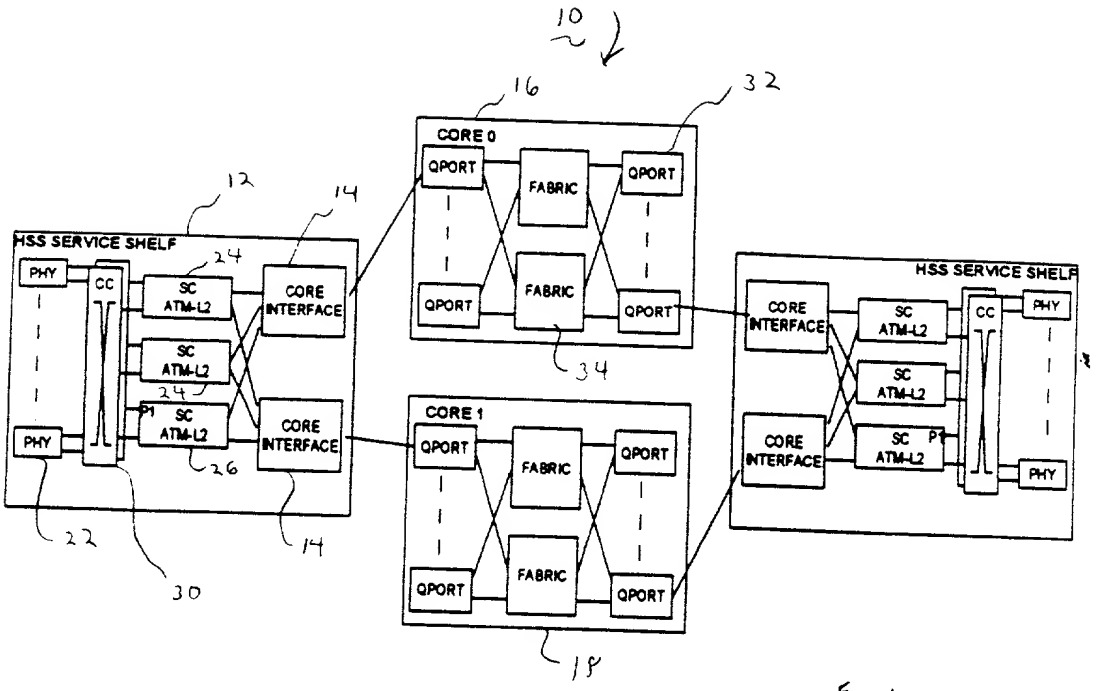

10
16
32
12
14
CORE 0
QPORT
FABRIC
QPORT
HSS SERVICE SHELF
24
PHY
CC
SC ATM-L2
CORE INTERFACE
SC ATM-L2
SC ATM-L2
CORE INTERFACE
PHY
26
22
30
14
34
CORE 1
HSS SERVICE SHELF
18

Fig 1

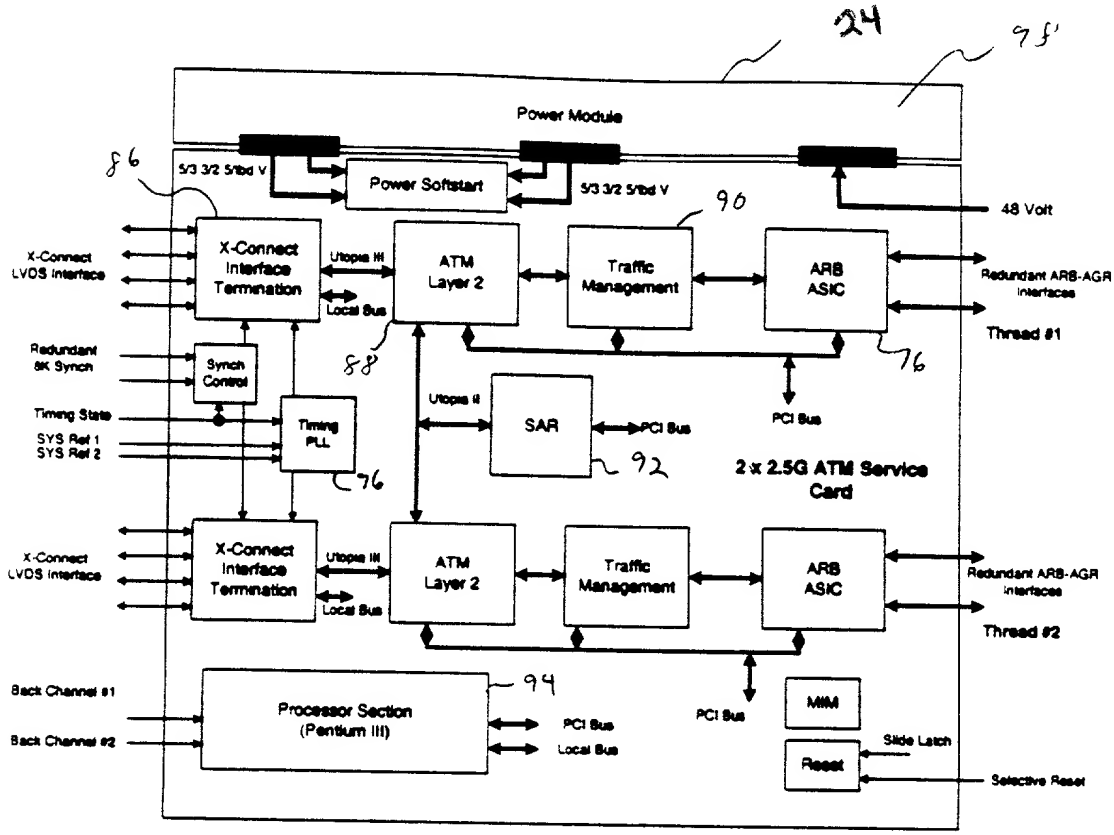

24
95
Power Module
86
5/3 3/2 5/bd V
Power Softstart
48 Volt
90
X-Connect LVDS Interface
X-Connect Interface Termination
Utopia III
Local Bus
ATM Layer 2
Traffic Management
ARB ASIC
Redundant ARB-AGR Interfaces
Thread #1
Redundant 8K Synch
Synch Control
88
76
Timing State
SYS Ref 1
SYS Ref 2
Timing PLL
Utopia II
SAR
PCI Bus
92
2 x 2.5G ATM Service Card
X-Connect LVDS Interface
X-Connect Interface Termination
Utopia III
Local Bus
ATM Layer 2
Traffic Management
ARB ASIC
Redundant ARB-AGR Interfaces
Thread #2
Back Channel #1
Back Channel #2
Processor Section (Pentium III)
94
PCI Bus
Local Bus
MMI
Reset
Slide Latch
Selective Reset

Fig 6

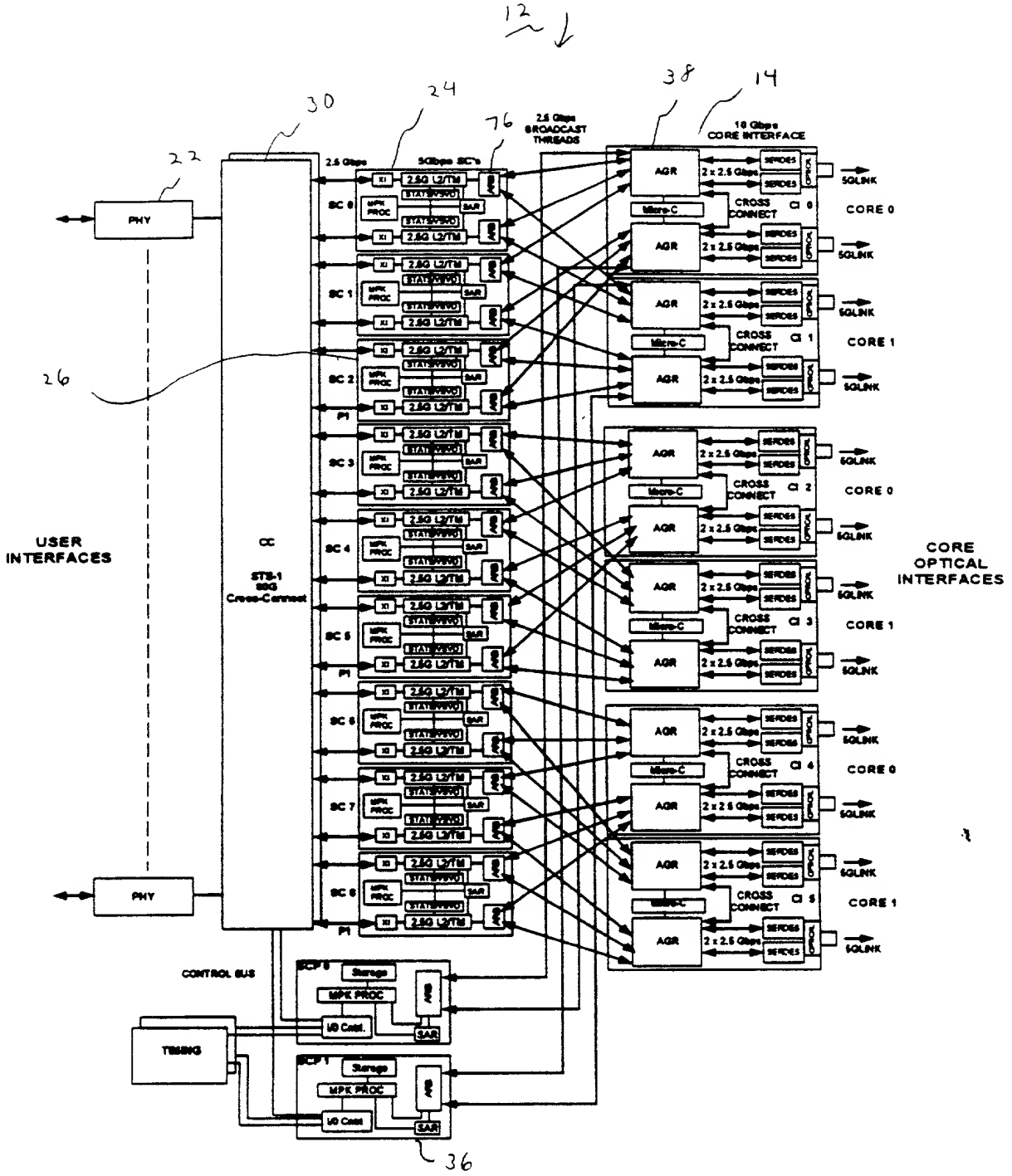

12
30
24
76
38
14
22
26
USER INTERFACES
PHY
PHY
CC
STS-1 80G Cross-Connect
2.5 Gbps
5Gbps SC's
2.5 Gbps BROADCAST THREADS
10 Gbps CORE INTERFACE
SC 0
SC 1
SC 2
SC 3
SC 4
SC 5
SC 6
SC 7
SC 8
P1
2.5G L2/TM
STATS/PERFO
MPK PROC
SAR
AGR
2 x 2.5 Gbps
SERDES
OPTICAL
Micro-C
CROSS CONNECT
CI 0
CI 1
CI 2
CI 3
CI 4
CI 5
CORE 0
CORE 1
5GLINK
CORE OPTICAL INTERFACES
CONTROL BUS
TIMING
SCP 0
SCP 1
Storage
I/O Cntrl.
36

Fig 2

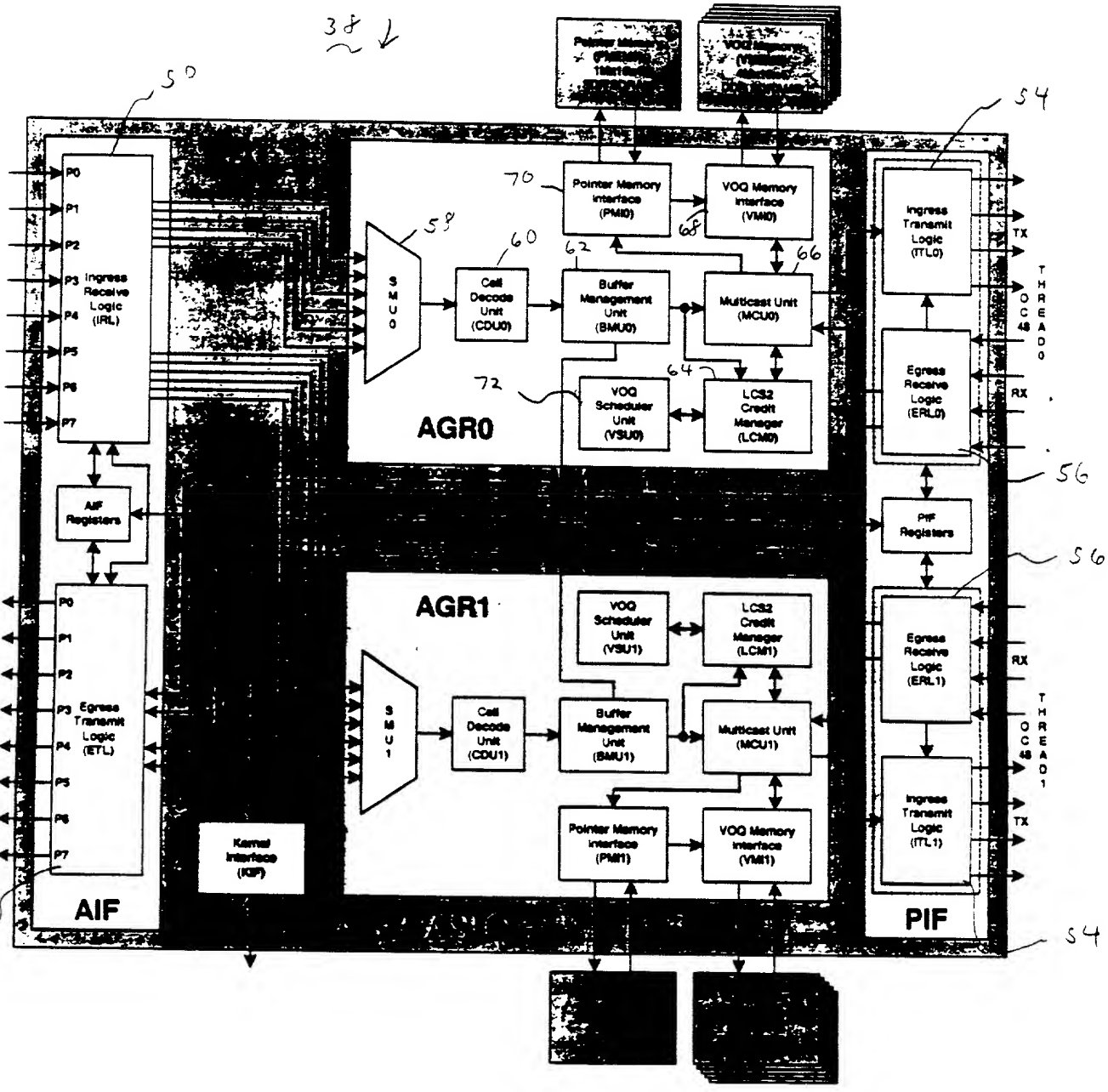
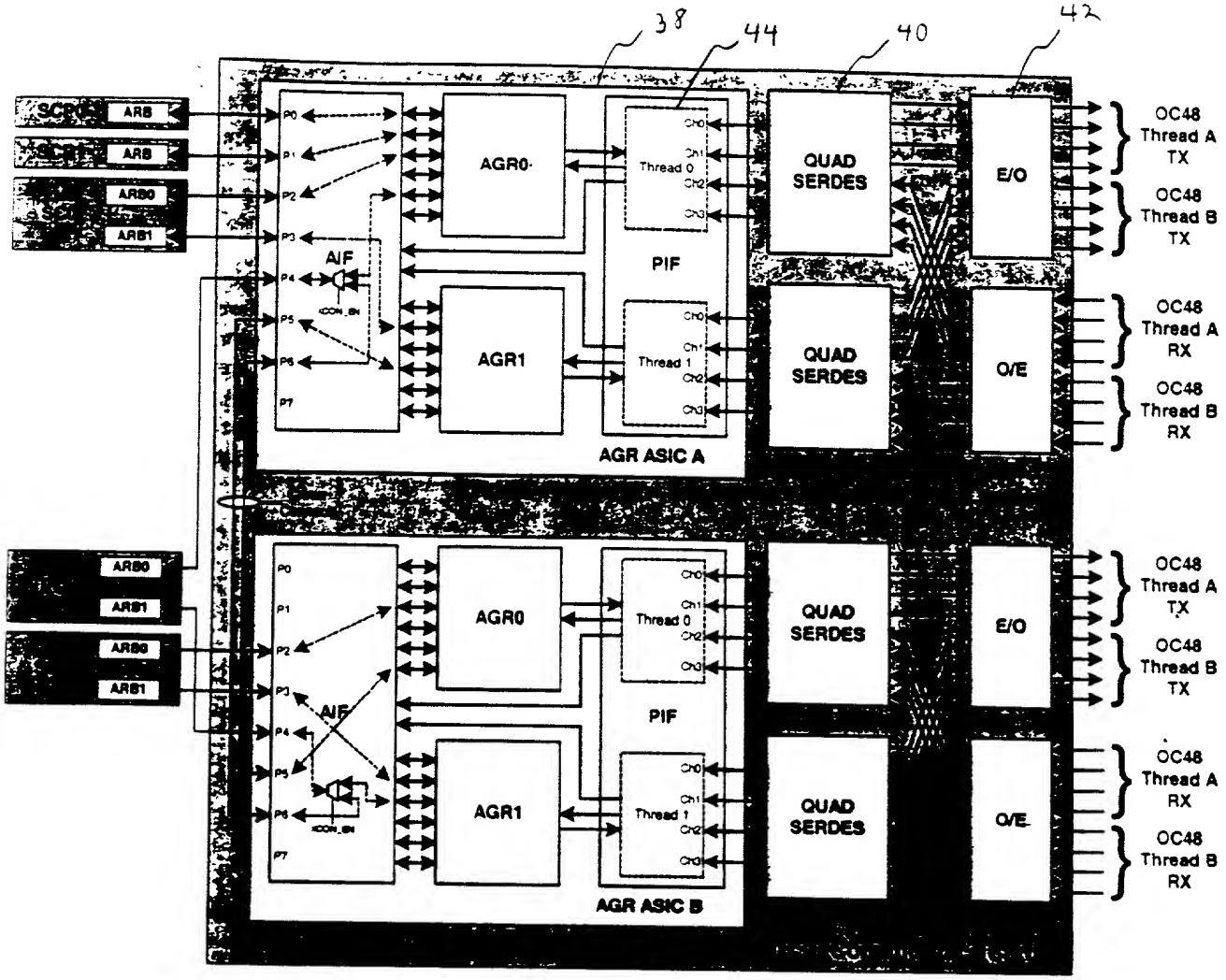

38
50
54
56
56
54
52
AIF
AGR0
AGR1
PIF
P0
P1
P2
P3
P4
P5
P6
P7
Ingress Receive Logic (IRL)
Egress Transmit Logic (ETL)
AIF Registers
Kernel Interface (KIF)
SMC0
SMC1
Cell Decode Unit (CDU0)
Cell Decode Unit (CDU1)
Buffer Management Unit (BMU0)
Buffer Management Unit (BMU1)
Multicast Unit (MCU0)
Multicast Unit (MCU1)
VOQ Scheduler Unit (VSU0)
VOQ Scheduler Unit (VSU1)
LCS2 Credit Manager (LCM0)
LCS2 Credit Manager (LCM1)
Pointer Memory Interface (PMI0)
Pointer Memory Interface (PMI1)
VOQ Memory Interface (VMI0)
VOQ Memory Interface (VMI1)
58
60
62
64
66
68
70
72
Ingress Transmit Logic (ITL0)
Ingress Transmit Logic (ITL1)
Egress Receive Logic (ERL0)
Egress Receive Logic (ERL1)
PIF Registers
TX
RX
THREAD 0
THREAD 1
OC 48

Fig 4


38
44
40
42
ARB
ARB0
ARB1
P0
P1
P2
P3
P4
P5
P6
P7
AIF
AGR0
AGR1
Ch0
Ch1
Ch2
Ch3
Thread 0
Thread 1
PIF
AGR ASIC A
AGR ASIC B
QUAD SERDES
E/O
O/E
OC48 Thread A TX
OC48 Thread B TX
OC48 Thread A RX
OC48 Thread B RX

14

Fig 3

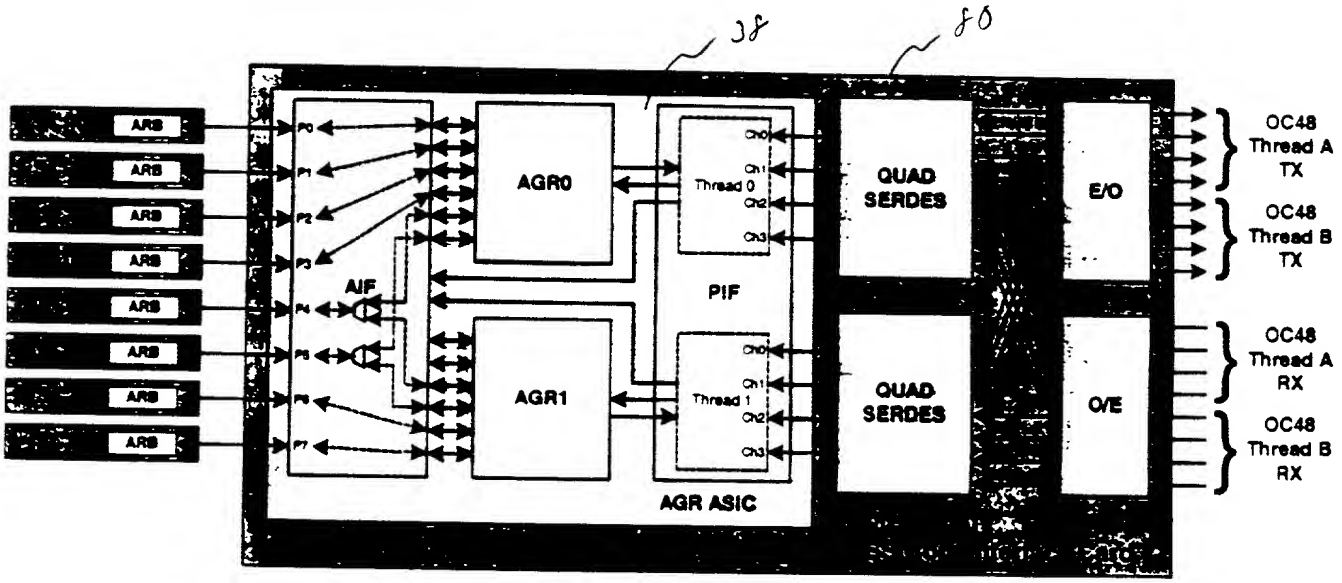

38
80
ARB
P0
P1
P2
P3
P4
P5
P6
P7
AIF
AGR0
AGR1
Ch0
Ch1
Ch2
Ch3
Thread 0
Thread 1
PIF
AGR ASIC
QUAD SERDES
E/O
O/E
OC48 Thread A TX
OC48 Thread B TX
OC48 Thread A RX
OC48 Thread B RX

Fig 5

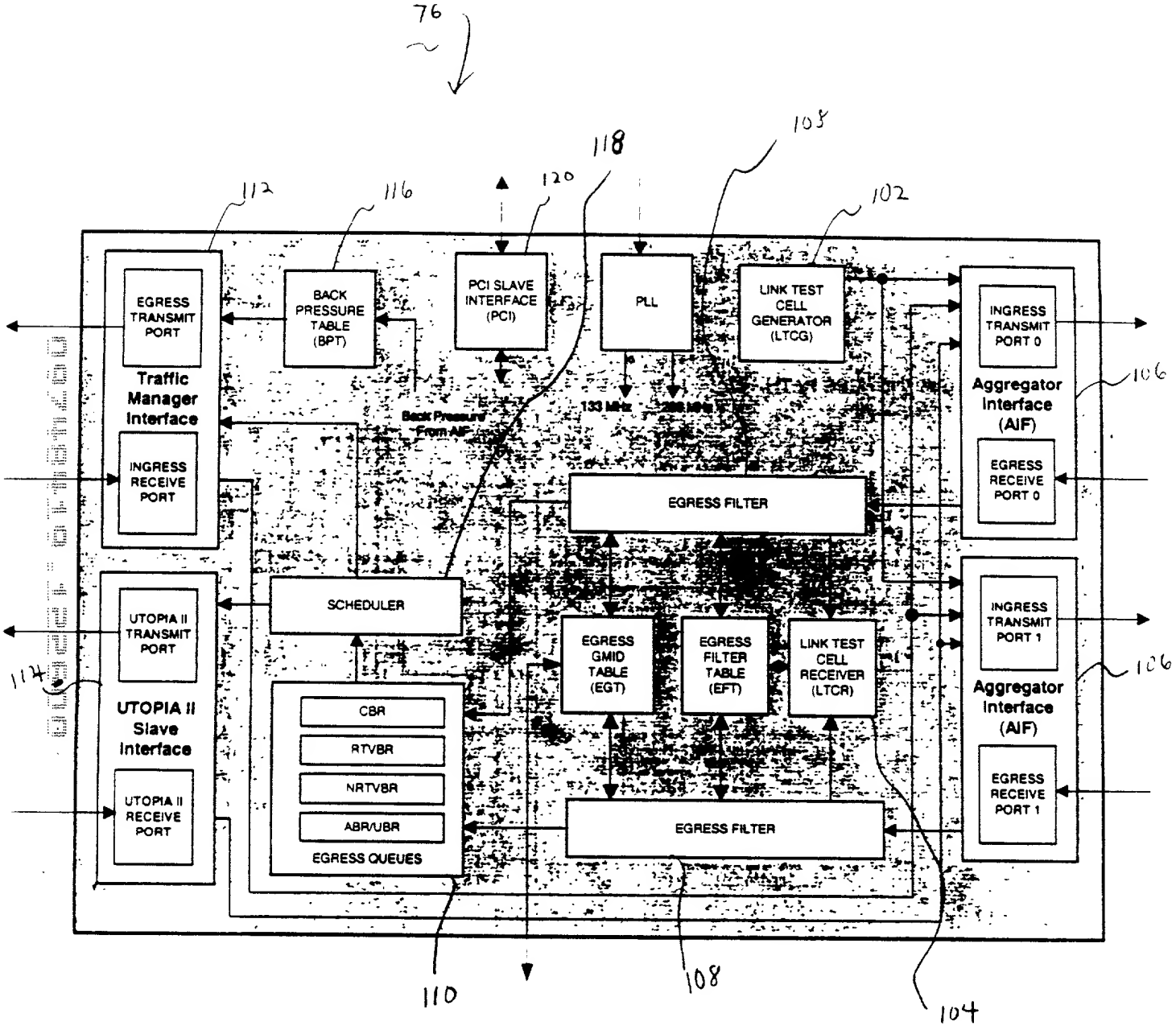

76
118
105
112
116
120
102
EGRESS TRANSMIT PORT
BACK PRESSURE TABLE (BPT)
PCI SLAVE INTERFACE (PCI)
PLL
LINK TEST CELL GENERATOR (LTCG)
INGRESS TRANSMIT PORT 0
Traffic Manager Interface
Back Pressure From AIF
133 MHz
Aggregator Interface (AIF)
106
INGRESS RECEIVE PORT
EGRESS RECEIVE PORT 0
EGRESS FILTER
SCHEDULER
UTOPIA II TRANSMIT PORT
INGRESS TRANSMIT PORT 1
EGRESS GMID TABLE (EGT)
EGRESS FILTER TABLE (EFT)
LINK TEST CELL RECEIVER (LTCR)
114
UTOPIA II Slave Interface
CBR
RTVBR
NRTVBR
ABR/UBR
EGRESS QUEUES
UTOPIA II RECEIVE PORT
EGRESS RECEIVE PORT 1
EGRESS FILTER
110
108
104

Fig 7

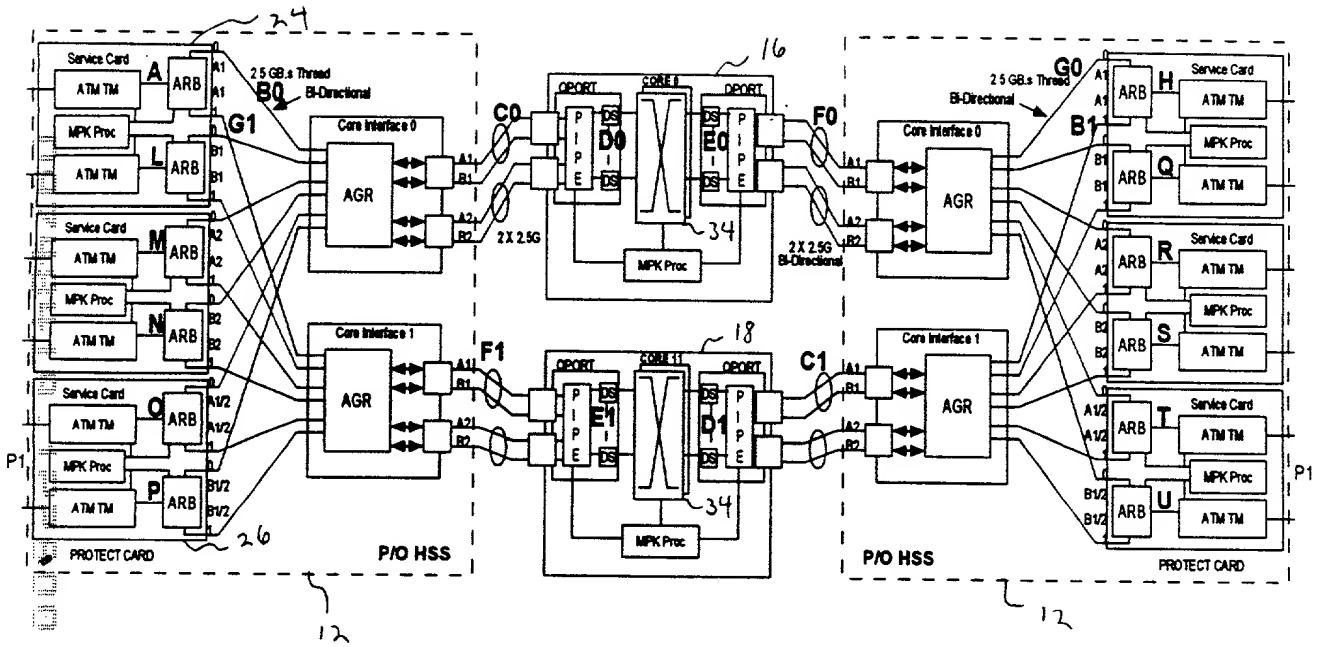


Figure 8 End to End Test Cell Flow, ARB<>ARB

LTC Generator Table

x.y (10 bits) Index (1K)	Enable TX for flow Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0	Pointer to next flow (10bits)
0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	
...	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	
1048	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	

LTC Generator Field Definitions

Field	Definition
Z7-Z0	Enable test cell generation for the particular Z flow. 1 = Send LTC on flow 0 = Do not set LTC on flow
Ptr	Point to next location or next flow in this table that contains test cell information to send.

Fig 9

LTC Receiver Table

x.y (10 bits) Index (1K)	Enable Check [7:0]	Enable Check [7:0]	Cell Rcvd [7:0]	Cell Rcvd [7:0]	Fault [7:0]	Fault [7:0]	Count [9:0]	Count [9:0]	Error Cnt [3:0]	Error Cnt [3:0]
	Core 0	Core 1	Core 0	Core 1	Core 0	Core 1	Core 0	Core 1	Core 0	Core 1
0	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxx	xxxx
...	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxx	xxxx
1023	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxx	xxxx

LTC Receiver Field Definitions:

Field	Definition
Enable Check	Enable test cell verification for that x.y.z.
Cell Rcvd	Set when a cell comes in on a flow. Cleared by table checker.
Fault	Set when a link is declared faulted, reset when a link is declared good.
Count	Start counting up when the table has been scanned and enable is set for a flow but a LTC has not been received on that flow. When the programmable threshold that indicates when to flag a flow as bad is reached, and interrupt will be generated to the processor interface. Any Z can be 'bad' for the count to increment for the x.y. When there are no errors after an error condition, this will start to count the number of good check cycles for a flow. After the programmable threshold that indicates when a flow is considered good is reached the flow is declared good and the processor is notified via an interrupt if enabled.
Error Cnt	Count of test cells with fixed payload errors.

Fig 10